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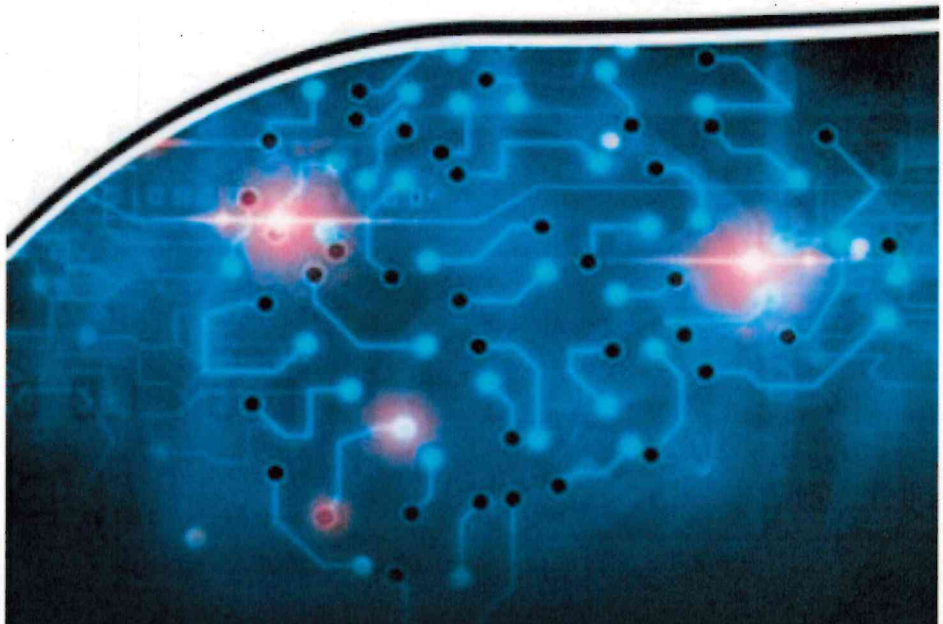

ELECTRONIC CIRCUIT ANALYSIS

Feim Ridvan Rasim
Michał Tadeusiewicz et. al

Electronic Circuit Analysis

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Contributors

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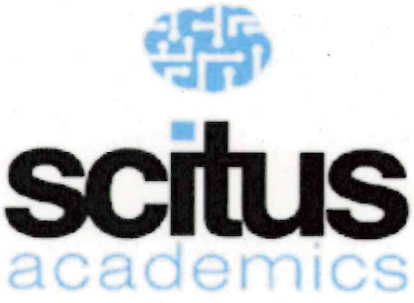

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Preface

Fault diagnosis of electronic circuits has been one of the most challenging topics for researchers and test engineers. Given the circuit topology and nominal circuit parameter values, fault diagnosis is to obtain the exact information about the faulty circuit based on the analysis of the limited measured circuit responses. Fault diagnosis of electronic circuits is essential for analog and mixed-signal systems testing and maintenance both during the design process and the manufacturing process of VLSI ASICs. With recent sharp development of electronic design automation tools and widespread application of analog VLSI chips and mixed-signal systems in the area of wireless communication, networking, neural network and real-time control, the interests in analog test and fault diagnosis revives. System-on-chip solutions favored by modern electronics pose new challenges in this topic such as increased complexity and reduced die size and accessibility. As discussed earlier, the conventional method for multiple fault diagnosis can be divided into three steps: fault detection, fault location determination, and finding the faulty elements values. This conventional method is readily deemed to be a numerical method by its very own nature but it is presented here as it provides basic insight to the problem and the limitations facing all numerical methods. While process engineers have traditionally coped with die-to-die fluctuations, the today within-die variations are more subtle since they imply that different areas of the same die exhibit different values of the various parameters.

Electronic Circuit Analysis provides state of the art complete coverage of electrical circuits and to the field of energy conversion technologies, analysis and design. A number of methods of analyzing power electronic circuits are discussed and illustrated. Chapters are contributed by worldwide authors and specialists to equip readers with necessary background material in such topics as devices, switching circuit analysis techniques, converter types, and methods of conversion.

Designed for senior undergraduate and graduate electrical engineering students, this book provides students with the ability to analyze and design power electronic circuits used in various industrial applications.

Chapter 1

Analysis of Electronic Circuits with the Signal Flow Graph Method

Feim Ridvan Rasim, Sebastian M. Sattler

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Abstract

In this work a method called "signal flow graph (SFG)" is presented. A signal-flow graph describes a system by its signal flow by directed and weighted graph; the signals are applied to nodes and functions on edges. The edges of the signal flow graph are small processing units, through which the incoming signals are processed in a certain form. In this case, the result is sent to the outgoing node. The SFG allows a good visual inspection into complex feedback problems. Furthermore such a presentation allows for a clear and unambiguous description of a generating system, for example, a netview. A Signal Flow Graph (SFG) allows a fast and practical network analysis based on a clear data presentation in graphic format of the mathematical linear equations of the circuit. During creation of a SFG the Direct Current-Case (DC-Case) was observed since the correct current and voltage directions was drawn from zero frequency. In addition, the mathematical axioms, which are based on field algebra, are declared. In this work we show you in addition: How we check our SFG whether it is a consistent system or not. A signal flow graph can be verified by generating the identity of the signal flow graph itself, illustrated by the inverse signal flow graph (SFG^{-1}). Two signal flow graphs are always generated from one circuit, so that the signal flow diagram already presented in previous sections corresponds to only half of the solution. The other half of the solution is the so-called identity, which represents the (SFG^{-1}). If these two graphs are superposed with one another, so called 1-edges are created at the

node points. In Boolean algebra, these 1-edges are given the value 1, whereas this value can be identified with a zero in the field algebra.

Keywords: Analog, Feedback, Network Theory, Symbolic Analysis, Signal Flow Graph, Transfer Function

1. Introduction

There are various methods in the circuit technology to calculate transfer functions of electrical circuits such as Kirchhoff's laws, two-port network theory, nodal analysis method [1] and time constant method [2]. These methods are generally time-consuming and computationally intensive. Moreover, it is always useful to develop a common graphical model, with using this model to make a connection between the state variables (parameters) and the transfer function as well as to obtain a better understanding of the complex functionality of a network. Using mesh rules, node rules and Ohm's equations a signal flow graph can be build. Targeted minimization of subgraphs, allows the calculation of a transfer function easier. In this paper we repeat the mathematical methodology for the symbolic analysis of real electronic circuits on the basis of a given real circuitry. It is based on graph theory, the so called SFG method. The signal flow graph (SFG) is a vividly method to present the internal structure of a system or the interaction of several systems. This presentation allows a better understanding of the function as well as the interrelations of one or more systems. Signal flow graphs are formally defined graphs [3]. Such a mapping enables a one-to-one (local-bijective) and understandable description of a generating system. It serves to increase clarity as well as contribute to an understanding of the circuit. The SFG allows a further comprehensible and simple visual consideration of the problem. It shows us all the functions of every part in the circuit and the connections between them. It is also a good method to help us to define the states in the circuit. It helps us to understand the circuit deeply and systematically. In addition, physical connections of the circuit become more recognizable. For the understanding of the circuit, the signal flow graph is a suitable method for the representation. To present the application we use a Common-X circuit as a use case. First, the Common-X circuit is split into its subcircuits and for each subcircuit their associated SFGs are established. Then by the superposition of the SFGs of the subcircuits the total SFG for the Common-X circuit results.

Organization of the paper: First, the theoretical foundations are briefly explained in Chapter 2. They are regarded as basic knowledge in order to understand this work. Subsequently, the implementation is described in detail in Chapter 3 and visualized by sketches and signal flow graphs. In the end, the results and the core outline of the work are summarized again and an outlook is given.

2. Theoretical Foundations

Signal flow graph: A signal flow graph describes a system by its signal flows by directed and weighted graph [3] [4] [5]. Similarly, an SFG provides a graphical representation of a set of linear relationships [3] [6] [7]. For this reason, a signal flow graph can be constructed between the materials using the Kirchhoff's laws, the current and voltage relationship. The directed and undirected graphs, the signals are applied to nodes and functions on edges; the direction is given by an arrow on the edge. The edges of the signal flow graphs are small processing units, through which the incoming signals are processed in a certain form. In this case, the result is sent to the outgoing node [3]. In network theory are often used ohmic resistors, capacitors and inductors. When considering these elements, the direction of the directed and weighted signal flow graph can not be interchanged easily. Prior to changing the direction of the arrow direction, the function on the edge has to be inverted. The material equation is given as an example. The signal flow graph with the respective function on the edge is shown in **Figure 1** [8].

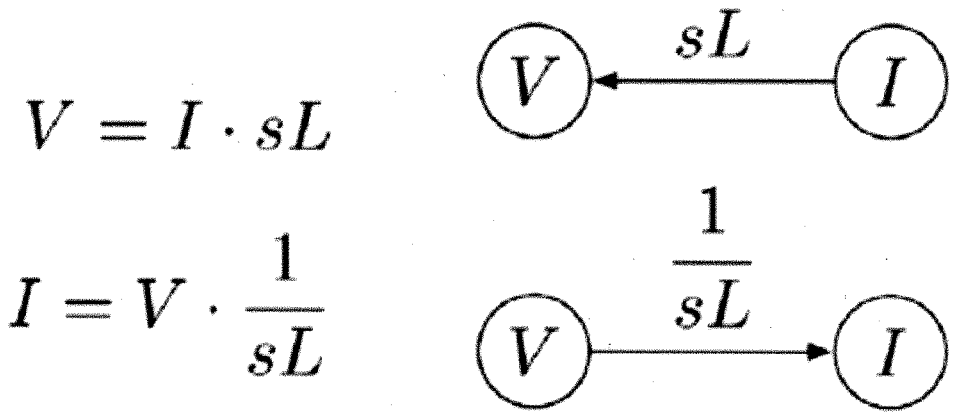


Figure 1. SFG of an inductance.

2.1. Elements of a Signal Flow Graph

A signal flow graph exists next to edges and nodes of paths, loops, input node and output node. A node is a point or a circle, which reproduces a signal or a variable. In order to illustrate these individual elements, the **Figure 2** is to be investigated in more detail.

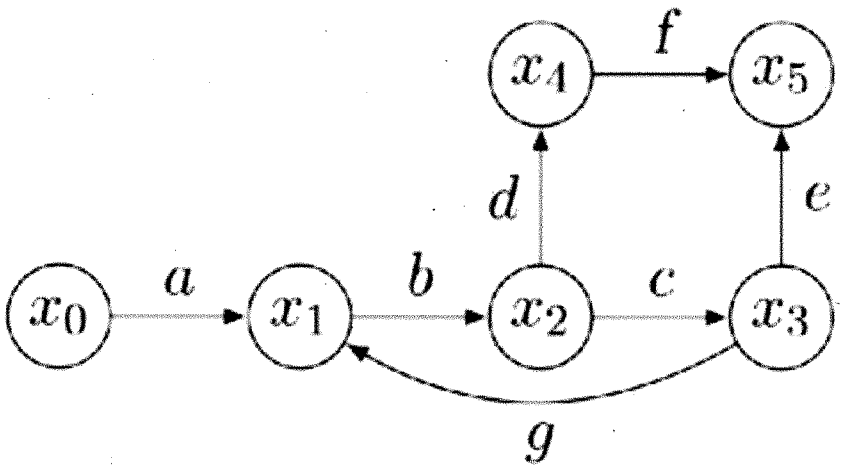


Figure 2. Example of a signal flow graph (SFG).

This signal flow graph has six nodes and seven edges. A node is a point or a circle that represents a signal or a variable. In the example, the variables x_1, x_2 etc. represent a node. There are different types of nodes. A dependent node has one or more leading incoming edges and any number of leading outgoing edges. Input node (x_0), also known as source node, has only outgoing paths and represent independent variables. An output node (x_5), also known as sink node, has only incoming paths and is in contrast to the input node a dependent variable. A path is a connected sequence of edges in one direction, the connection of x_1 to x_3 by edges *b,c* via node x_2 represents a path. The path gain is the product of the functions on the edges along a path. In this example, the path gain is $b \cdot c$. A reverse path is a path that leads towards the entrance node. As with the forward path, the nodes can only be passed once. The connection via the edges *b,c* and *g* build a feedback loop, the initial loop is x_1 in this case. A feedback loop is present when the start and end nodes are the same. When the edges *b,c* and *g* pass through, we reach the original node x_1: $x_1 \rightarrow x_2 \rightarrow x_3 \rightarrow x_1$. Loops are equal oriented edges forming a closed path and will touch no node multiply. A self-referential loop is exactly present when a path flows from one node in the same node without crossing other nodes [9].

2.2. Modifications of Signal Flow Graph

By **associative law** (**Figure 3**) sequential edges can be summarized. As soon as three nodes which are interconnected via a path so present, that there are the $x_0 \rightarrow x_1 \rightarrow x_2$ connected, the central node x_1 is eliminated from the graph:

$$x_0 \cdot a = x_1, x_1 \cdot b = x_2 \Rightarrow x_0 \cdot a \cdot b = x_2$$

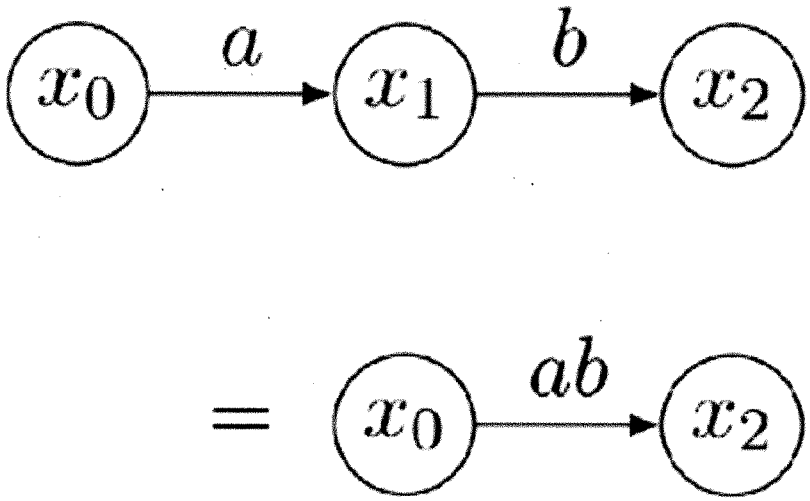


Figure 3. Summary of sequential edges-associative law.

Parallel running edges with the same input node x_0 and output node x_1 can be combined with the **distributive law** (**Figure 4**). The resulting graph is minimized to an edge. For example, two edges from node x_0 flow into the node x_1. Algebraically, the node x_1 be expressed as:

$$x_0 \cdot a + x_0 \cdot b = x_0 \cdot (a + b) = x_1$$

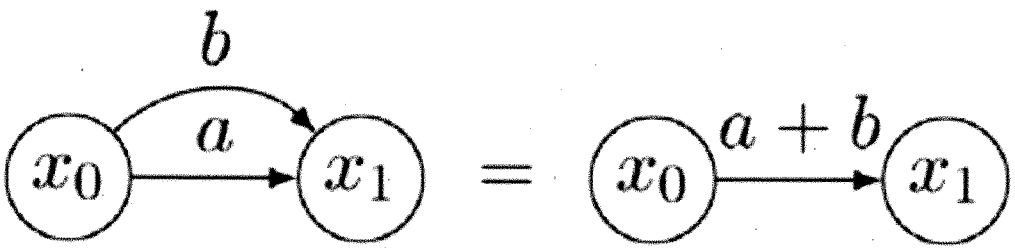


Figure 4. Summary of parallel edges-distributive law.

Dissolving a feedback loop (**Figure 5**): In order to eliminate the node x_1, be first the functions multiplied on the edges along the forward path. Next, forming the product of the individual loop gains. This is the signal flow graph of two edges $a \cdot b$ and $c \cdot b$, in which $c \cdot b$ is a self-referential loop. Thus, the node x_1 is removed from the graph and the feedback has been summarized in a reflexive edge:

$$x_0 \cdot a = x_1, x_1 \cdot b = x_2 \Rightarrow x_0 \cdot a \cdot b + x_2 \cdot c \cdot b = x_2$$

$$\Rightarrow x_0 \cdot a \cdot b = x_2 (1 - c \cdot b) \Rightarrow x_0 \frac{a \cdot b}{1 - c \cdot b} = x_2$$

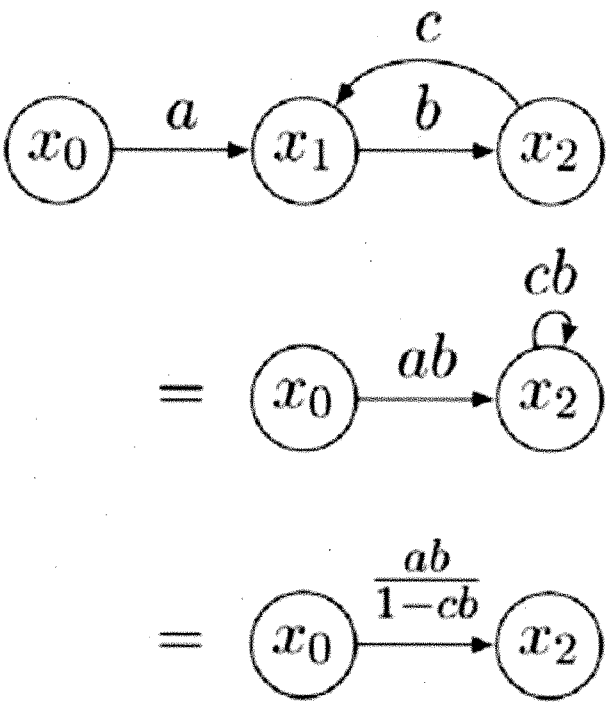


Figure 5. Dissolving a feedback loop.

A reflexive edge (self-referential loop) can be eliminated, in which one by one divides the product of the functions on the edges toward the reflective edge minus the product of the functions on the reflexive edges. For more reflexive edges one can use the same procedure. In **Figure 6**, the reflexive edge resolved is shown with the corresponding weights [4] [6].

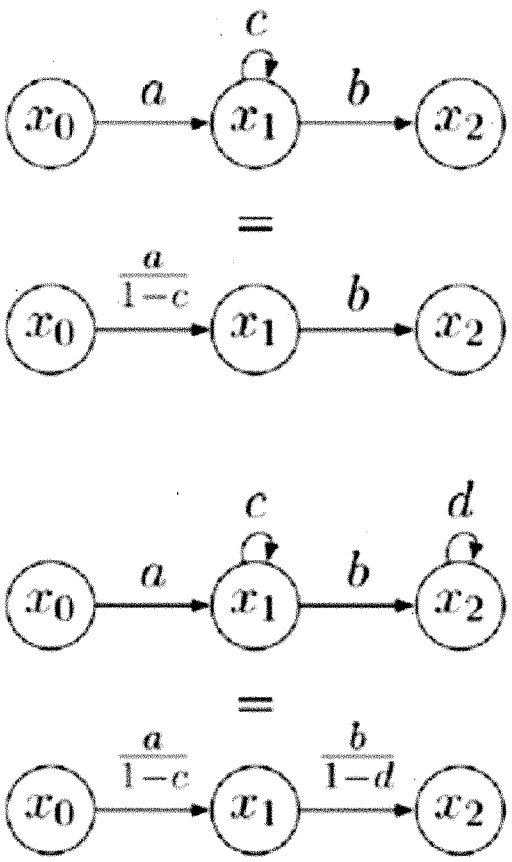
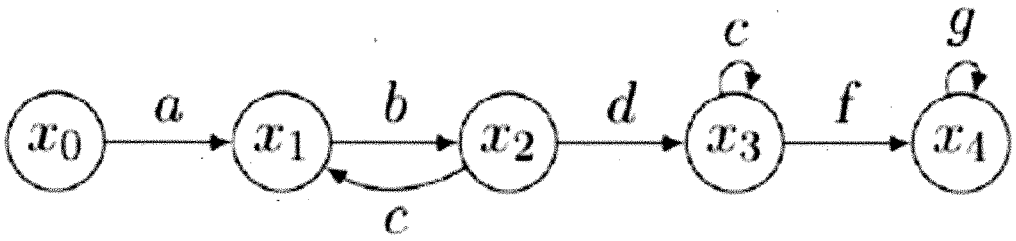


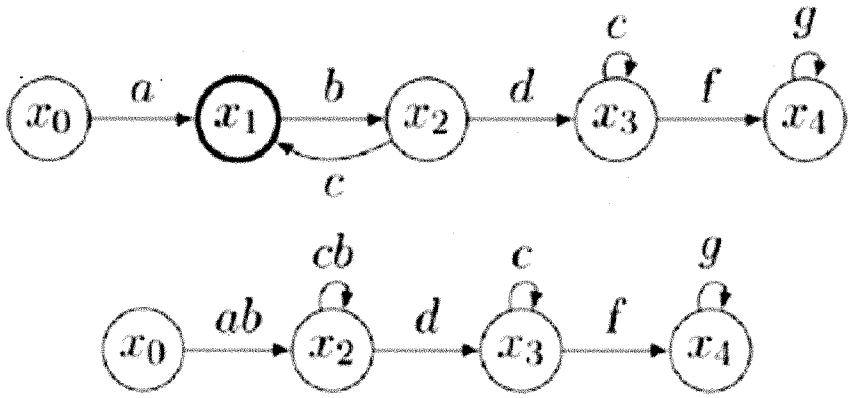
Figure 6. Dissolving a reflexive edge.

Example:

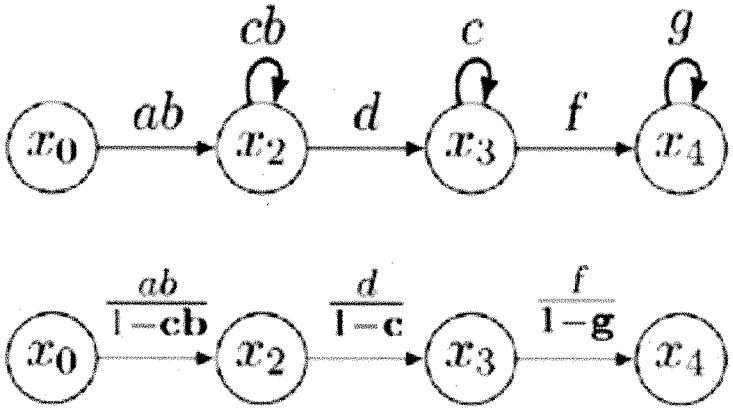


- Source node x_0
- Sink node x_4
- Target: Simplification of the SFG consists only of start and end nodes
- Transfer Function G

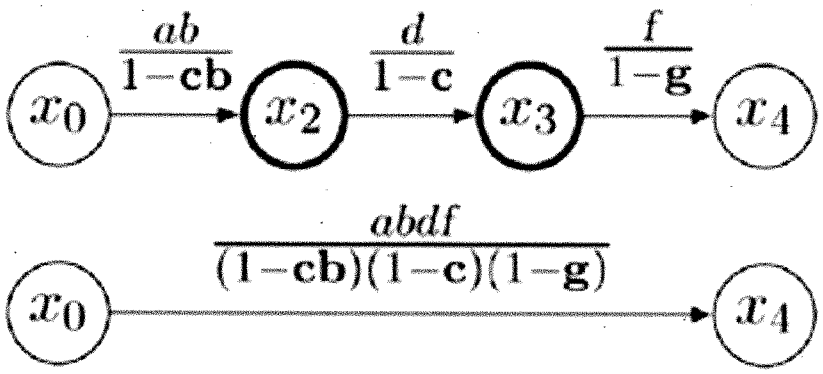
1) The node x_1 is to be eliminated: Resolving a feedback loop.



2) Eli4mination of reflexive edges:



3) On the basis of the associative law, the nodes x_2 and x_3 are taken from the graph:



$$G = \frac{x_4}{x_0} = \frac{a \cdot b \cdot d \cdot f}{(1 - c \cdot b)(1 - c)(1 - g)}$$

3. Analysis of Common X-Circuit

In this section, we will show you an example: How to set up the SFG, then by using SFG modification rules how to simplify the SFG to calculate the transfer function, and additionally how we check our SFG whether it is a consistent system or not?

The Common X circuit (**Figure 7**) is chosen as an example of the determination of the signal flow graph in the course of work. Therefore, at this point the members of the small-signal model are explained: V_{in} is the input voltage, V_L is the output voltage, R_Y is a lead resistance or the internal resistance of the voltage source, r_p the baseband resistance of a BJT, g_m is the transconductance or the steepness of the CX circuit with $g_m = i_{out}/V_{in}$. To apply now the method SFG, the circuit is divided into partial circuits (**Figure 8**). The intention in the division is to reduce the complexity of the analysis and to win by the substeps a better and clearer view of the functioning of the structure. The small-signal equivalent circuit diagram of the CX circuit can be divided into two parts following circuits: In order to simplify the effort of calculation, in the first step the circuit is broken. This results in two subcircuits.

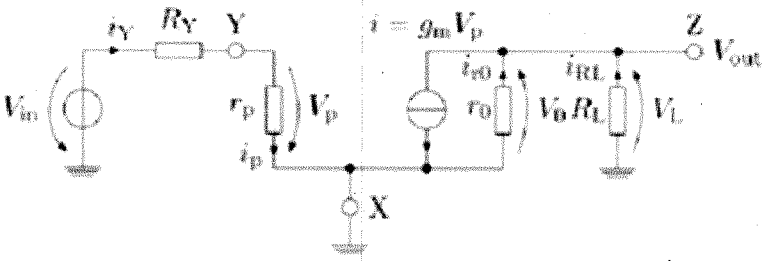


Figure 7. Small signal equivalent circuit of the CX-circuit.

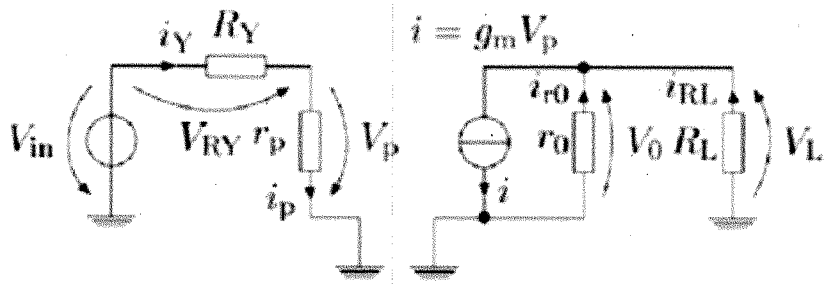


Figure 8. Small signal equivalent circuit of the CX-circuit in separate form.

3.1. Analysis of First Subcircuit

The first subcircuit is a simple voltage divider. Based on the above considerations (**Figure 8**) can now be derived for the first subcircuit of the signal flow graph (**Figure 10**). Before the signal flow graph is derived from the first subcircuit, the first subcircuit is to be simplified by a further step. If the resistor R_Y is taken out of the circuit, then a circuit with an ideal voltage source and a resistor is r_p obtained, **Figure 9**. In the ideal case, the total voltage V_{in} drops across the resistance r_p. The voltage source supplies the current i_p as a function of the resistance r_p. A voltage source should never be confused with a power source. The voltage source provides a current dependent on the load. On the other hand, the current source provides a constant current independent of the load. The mesh rules and the material equation yield the equations:

$$V_{in} =: V_p \text{ with } i_p := V_p \cdot \frac{1}{r_p}$$

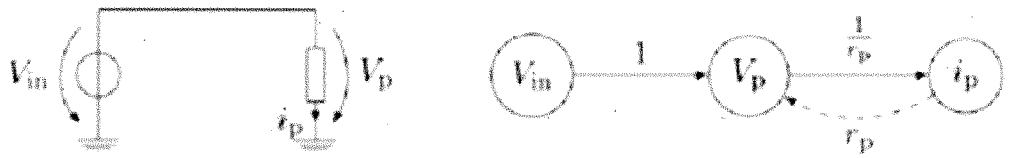


Figure 9. First subcircuit (left) of the CX-circuit is simplified by R_Y and SFG (right) of the circuit.

Thus, the signal flow graph can be reproduced for this simple structure. The dashed edge completes the identity of the signal flow graph. Therefore, the signal flow representation represents only a half of the solution. For each material equation, we can go back, **Figure 9**. On the basis of the previous considerations, the signal flow graph for the first sub circuit can now be derived much more easily. It is desirable that the total voltage V_{in} of the voltage source drops across the resistor r_p. In reality, however, a small part of the voltage at the much smaller resistance R_Y drops. The desired voltage at the resistor r_p can thus be adjusted with the resistance R_Y. Thus, the mesh equation for the first sub-circuit can be established:

$$V_p := V_{in} - V_{RY}$$

Depending on the resistance r_p is generated by the voltage V_p of the current i_p. The material equation is:

$$i_p := V_p \cdot \frac{1}{r_p}; \quad V_{RY} := i_Y \cdot R_Y; \quad i_p =: i_Y$$

The current i_p flowing through the resistor R_Y and generates the voltage V_{RY}. Thus, the signal flow graph of the first partial circuit may be formed by expansion of the signal flow graph of the ideal case without R_Y. This only needs around the edge (i_Y, V_{RY}) of the circuit to be supplemented. The dashed edges complement the axiomatic identity of the signal flow graph (**Figure 10**).

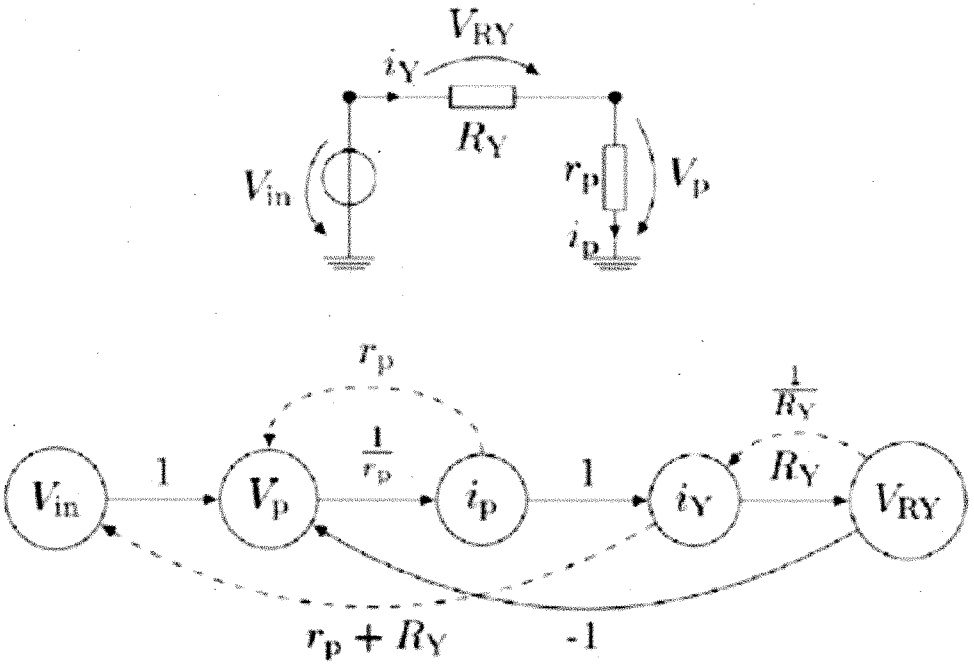


Figure 10. First subcircuit (above) of the CX-circuit and SFG (below) of the first partial circuit.

3.2. Analysis of Second Subcircuit

When dividing the common X-circuit, the second subcircuit between the nodes X and Z forms in **Figure 12** a current divider. Analogously to the first subcircuit, the current divider is initially to be considered for the sake of simplicity without the resistor r_p, **Figure 11**. In the ideal case, the source current i should flow completely through the load resistor R_L and generate the voltage V_L there. A current source should not be confused with a voltage source. The current source i supplies a current which is independent of the

load resistor R_L. By these statements the equations of the currents and the material equations can be defined for this simple case.

$$i =: i_{RL}; V_L := i_{RL} \cdot R_L$$

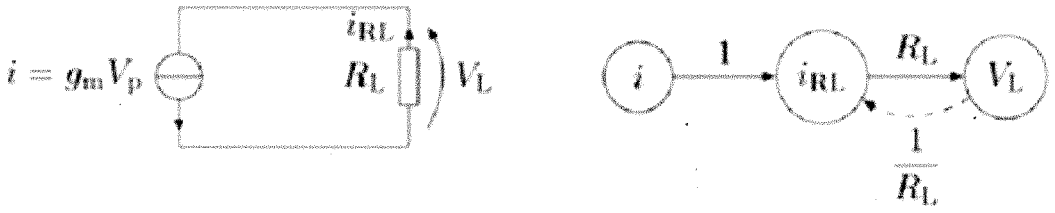


Figure 11. Second subcircuit (left) of the CX-circuit is simplified by r_0 and SFG (right) of the circuit.

From the definitions, the signal flow graph for the circuit of **Figure 11** (left) can be constructed. The dashed edges describe the identity of the signal flow graph. With the help of the circuit from **Figure 11**, the signal flow graph of the second subcircuit can be determined much more easily. In reality, however, the total current i of the source does not flow through the load resistor R_L. In order for the entire current i to flow through the load resistor R_L, the resistance r_0 would have to be infinite. But since the resistance r_0 is not infinite, a small fraction of the source current flows through it. The current i_{RL} through the load resistor R_L can be adjusted by a suitable choice of the resistor r_0. This allows the node rule to be set up.

$$i_{RL} := i - i_{r0}$$

The current i_{RL} generates the voltage V_L at the load resistor R_L, which is equal to the magnitude of the voltage falling to r_0. This relationship can be understood by means of the mesh rule. The voltage across the resistor r_0 produces the current i_{r0} which acts on the current i_{RL} through a negative feedback. In summary, the node, mesh rule and the material equations for the second subcircuit can now be set up.

$$i_{RL} := i - i_{r0}; \quad i_{r0} := V_0 \cdot \frac{1}{r_0};$$

$$V_L =: V_0; \quad V_L := i_{RL} \cdot R_L$$

If the signal flow graph of the simple circuit is extended by the nodes V_0 and i_{r0} using the above equations, the signal flow graph of the second subcircuit

will result, **Figure 12**. The material equations can be inverted. In reality, not all of the current i of the source flows through the load resistor R_L: Thus, if the total current i flows through the load resistor R_L, the resistance r_0 would be infinite. But the resistance r_0 being not infinitely large, a small portion of the source current flows through it. The current i_{RL} through the load resistor R_L can be adjusted by the appropriate choice of resistance r_0 or reduced by this resistance. Thus, the nodes usually can be placed. The current i_{RL} generates at the load resistor R_L the voltage V_L which is equal to the voltage drop across r_0. With the mesh analysis, this relationship can be traced. The voltage across resistor r_0 generates the current i_{r0} which acts back to the current i_{RL} through a negative feedback. In summary, the node, mesh and the material equations for the second subcircuit can now be set up. Extending the signal flow graph of the simple circuit around the edge (V_0, i_{r0}), yields the signal flow graph of the second subcircuit. The material equations can be inverted.

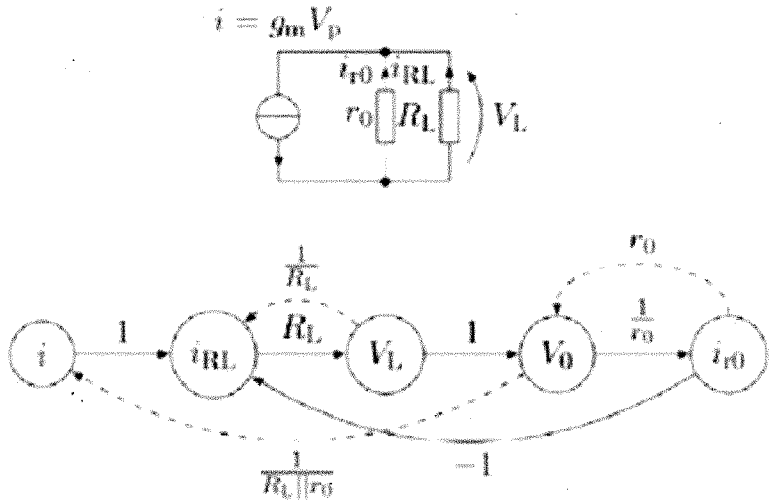


Figure 12. (Above) Second subcircuit of CX-circuit and (below) SFG of the second subcircuit.

3.3. Signal Flow Graph of Total CX-Circuit

To make the signal flow graph of the CX-circuit, the individual subgraphs must be combined into a graph (**Figure 13**). The current source i is a voltage controlled current source. It is controlled by the voltage V_p, the current is determined by $i = g_m \cdot V_p$. Following the relationship between the current source i and the voltage V_p the two signal flow graphs can now be interconnected, V_m as source, i_{RL} as sink, i_p and V_L as states.

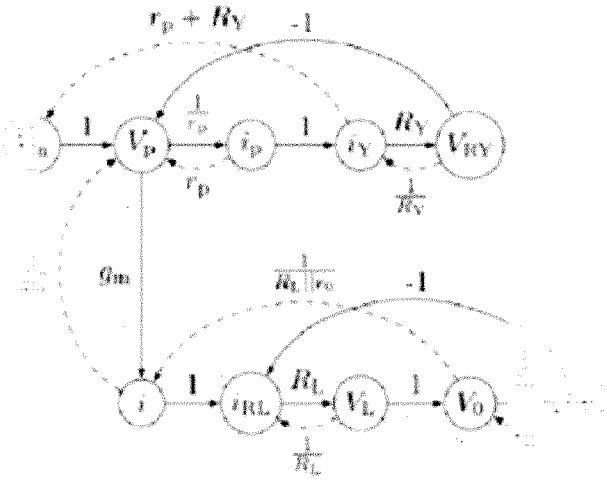


Figure 13. Signal flow graph of the total CX-circuit for $r_p \to \infty$ and $R_L \ll r_0$.

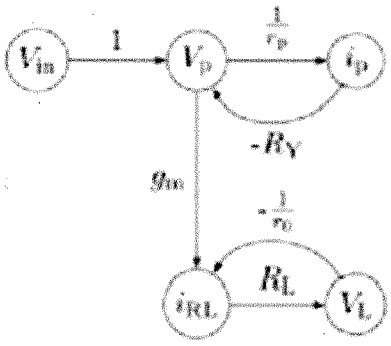
3.4. Transfer Function of CX-Circuit

3.4.1. Verification of the transfer function

Simplifying the signal flow graph in **Figure 13** using the SFG method. In order to find the transfer function, the signal flow graph from **Figure 13** is to be simplified step by step so that the individual loops and paths leading to the solution are clearly visible.

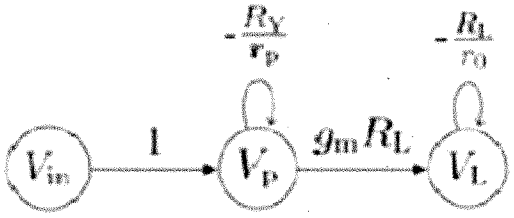
- Elimination of the nodes i_p, V_{RY}, i, V_0 and i_{r0}

Nodes (i_p, V_{RY}, i, V_0, i_{r0}) are eliminated by the associative law.



- Elimination of the node i_{RL}

The node i_p is removed from the graph using the associative law. The node i_{RL} is controlled by the rule for resolving feedback loops from the graph.



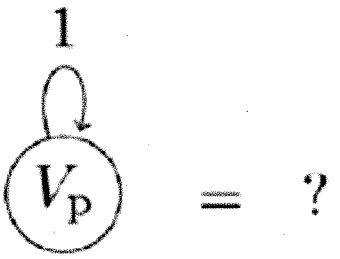
- Elimination of the reflexive edges and the node V_P

There is only one forward path from V_{in} to V_L

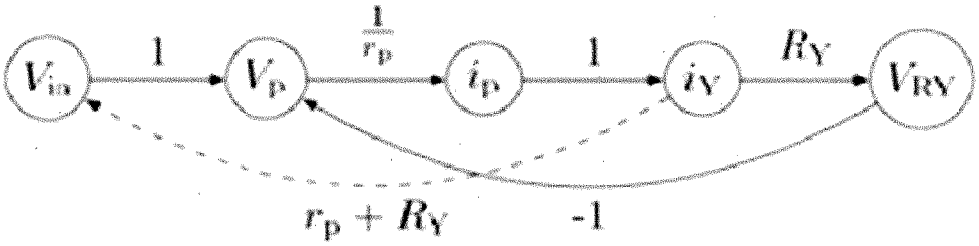
3.4.2. Proof of Method

How we check our SFG whether it is a consistent system or not? The mathematical axioms of our SFG are based on field algebra. If we look at all incoming and outgoing edges of a node, a super edge appears and this is a 1-edge. With 1-edges, we can check wheather this is a consistent system or not and the formula is graphically checked. Proof of the SFG method using the inverse signal flow graph (SFG^{-1}): A fundamental step at the end of each analysis process is to check whether the signal flow graph and the other representation analysis methods of a circuit developed therefrom have been correctly calculated. On the basis of this proof, it is determined whether the respective signal flow graph corresponds to a consistent system. A signal flow graph can be verified by generating the identity of the signal flow graph, illustrated by the inverse signal flow graph (dashed 1-edge). Two signal flow graphs are always generated from one circuit, so that the signal flow graph already presented in previous sections corresponds to only half of the solution. The other half of the solution, the so-called identity, which is represented by a dashed edge, represents the inverse signal flow graph (SFG^{-1}). If these two graphs are superposed with one another, so-called 1-edges are created at the node points. In Boolean algebra, this 1-edge is given the value 1, whereas this value can be identified with a zero in the field algebra.

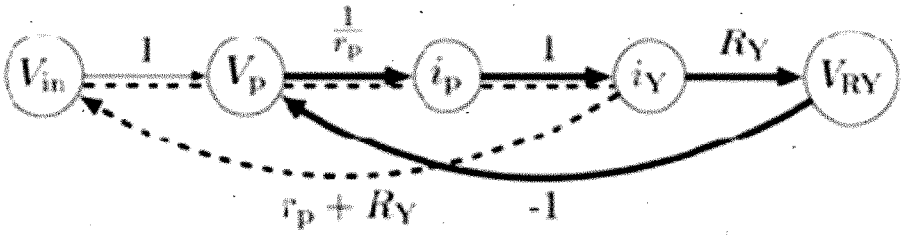
Example: We want to check the 1 edge of the node V_p.



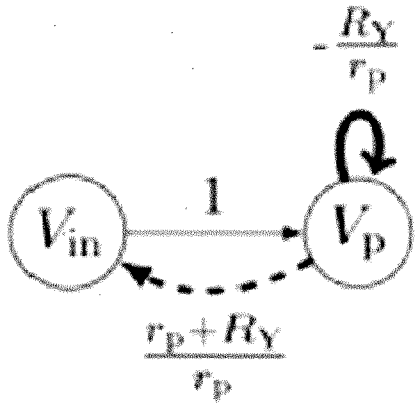
Now we look at all incoming and outgoing edges of this node of **Figure 13**, all other nodes and edges can be eliminated as well as dashed edges with material equations. Because material equations give us 1-edges, we do not use this to check. First we simplified **Figure 13** as follows.



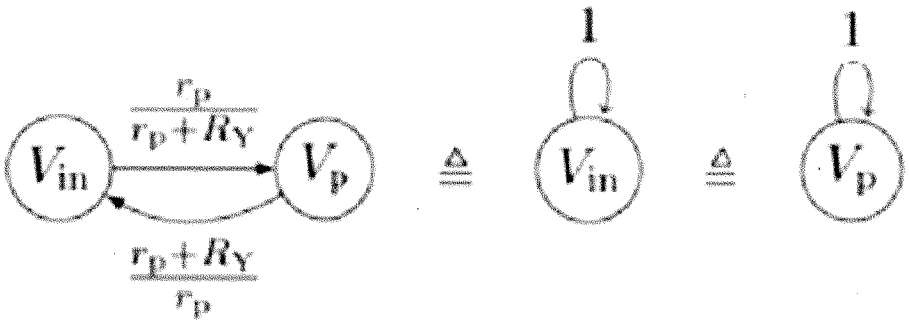
Then we look for incoming and outgoing edges within the loops. There are 2 loops, $V_P \to i_p \to i_Y \to V_{RY} \to V_P$ and $V_P \to i_p \to i_Y \to V_{in} \to V_P$, they are marked with diferent lines.



The nodes (i_p, i_Y, V_{RY}) are eliminated by the associative law. This gives the following signal flow graph.



Further simplification of SFG: Elimination of reflexive edges of V_p and then elimination of the reflexive edges of V_{in}. It gives us the 1 edge of the node V_p.



And finally our SFG is checked. Analogously we can use this proof method for all nodes.

Conclusion

The SFG analysis can offer a faster and more effective alternative to complex structures with the right approach and solution patterns. However, the signal flow graph represents only a projection of the solution of the network equations. Together (superimposed) to the inverted solution of the system is then obtained as a result all the states of the structure with self-imposed and unweighted loops. For the analysis of a network the SFG-method provides an important alternative, since you are saving in complex systems not only long calculus, but also get a most suitable overview in the interaction of the system components and spare parts. The method is rarely used, and the existing literature on the subject is little. One can always encounter various

problems in the analysis of a circuit that can now be easily understood with the knowledge of this method and verified. The key of understanding a circuit is always its real structure (physics). The SFG is the structure faithful model which brings together real physics and underlying theory. For understanding the cicuit, the signal flow graph is the most suitable representation. Thus the method can describe a generating system intelligibly and unambiguously. In this respect, the physical connections of a circuit are also more recognizable. Such a graph determines how a circuit works and shows what needs to be seen, which can not be fulfilled by the circuit diagram. It also makes a circuit reproducible and traceable. The fact that an SFG belongs to a model representation proves itself to be more compact and clearer. In addition, mathematical connections are illustrated more clearly due to the visualization, and certain computational steps are explained in a more comprehensible manner. As far as time is concerned, a very small computation time can be achieved with the aid of the SFG using the smallest memories. The SFG offers further great advantages. Since an SFG is compressible, only a small amount of material is required, so that the cost factor can be minimized. In addition, the method shows the highest quality since the SFG is directed and exhibits due to the 1-edges and the ability of being self-verifying. Despite this, the signal flow graph method still requires a high degree of research. This need relates, among other things, to the obstacles and difficulties that may arise when programming the graphics.

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Chapter 2

A Method for Finding Multiple DC Operating Points of Short Channel CMOS Circuits

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Abstract

This paper is devoted to the analysis of CMOS transistor circuits, fabricated in nanometer technology, having multiple DC operating points. The MOS transistors are characterised by the intricate PSP 103.1.1 model elected by the CMC as a standard. To find the operating points an approach is proposed based on a mathematical concept called a deflation. According to this concept the equations describing the circuit are deformed to avoid the solutions earlier determined and retain the remaining solutions. A new efficient deflation technique is developed and combined with the homotopy method and the discrete circuit equivalent of the Newton–Raphson nodal analysis. An algorithm has been worked out for finding multiple DC operating points of CMOS circuits encountered in practical applications. To illustrate the proposed approach three numerical examples are given.

Keywords: CMOS circuits, DC analysis, Deflation technique, Multiple operating points.