uC-Based ATE for Testing a DUT provided with Real-World Failure Models

Gürkan Uygur, Wolfgang Magerl, Wolfgang Sörgel, Sebastian M. Sattler
Chair of Reliable Circuits and Systems, LZS, Friedrich-Alexander-University Erlangen-Nuremberg
Paul-Gordan-Str. 5, 91052 Erlangen, Germany
Email: {guerkan.uygur,wolfgang.magerl,wolfgang.soergel,sebastian.sattler}@fau.de

Abstract

We present our prototype ATE solution for testing a device of elementary digital as well as analog functions provided with real-world failure models as a jumper construction. A modeled open circuit failure is done by unplugging the (normally plugged) respective jumper, and analogously a modeled short circuit failure is done by plugging the (normally unplugged) respective jumper. The DUT is supplied by a current limited voltage power supply. The programmable current limitation activates the overcurrent relay to protect the device in case of short circuit failure. The ATE resources for stimuli, measure and test evaluation are provided by an adequate uC-Board with programmable analog-to-digital io-channels. The test automation is implemented by the firmware of the uC, which corresponds to the test program of a conventional ATE including the pin-mapping, the test function library and the test flow (schedule). With this in mind, we are speaking about the Micro-ATE (uATE).

Within the use case above, we discuss the challenge for localization of the so called dominated (dominent) faults, which are not detectable uniquely due to the dominating faults within the scope of the stuck-at failure modeling. At this case the testing accuracy has to be enhanced. We solve this problem definition by deploying external current sources to provide additional stimuli at the given test points. Our approach results in the overall data modeling, which covers the test tree, the test flow, and the diagnose flow for fault localization.

Index Terms—ATE, uC-Board, stuck-at, dominating vs. dominated fault, testing accuracy, data modeling, test tree, test flow, diagnose flow, fault localization

1 Introduction

AUTOMOTIVE is increasingly developing into a modular, distributed, dynamic discrete event system with complex requirements specification and high demand on safety. Further, the automotive technology increasingly profit from the Integrated Circuit (IC) technology, which bundle analog-to-digital functionality with high efficiency and quality at low cost. For instance, IC Insights reports the $2013 - 2018$ automotive IC market Compound Annual Growth Rate (CAGR) of $10.8\,\%$, which is four percentage points greater than the next closest category of communications at $6.8\,\%$ [1]. It also highlights that Analog ICs and Microcontroller (uC) Units remain the two largest IC product categories within the automotive IC market [1]. Avionics and bio-medical systems are further safety-critical applications with steadily growing deployment of IC components [2].

Design and technology are more and more reaching their limits, so that simulation based validation is incapable to cover all possible scenarios, which is an unacceptable foundation, especially for safety critical systems [3]. Hence, it is well known that widely established simulation techniques are not by themselves adequate to ensure the correctness of complex systems [4]. The alternative is to employ theoretically sound formal verification and test [5]. Due to the increasing complexity of structure and functionality also the test of the real-world structure becomes more and more complex, hence the formal assignment between the (virtual) functionality and the (real-world) structure becomes more and more critical. This results in a high effort for design verification and test such that specification-oriented testing is getting more and more under pressure. This constellation leads to an ever-increasing challenge particularly regarding safety critical circuits and systems.

Within the laboratory conditions, the Test Environment (TE) could primarily be equipped with general purpose hand-held devices like voltmeters as well as oscilloscopes. For automated manufacturing testing of a Device Under Test (DUT) cost-prohibitive (monolithic) Automated Test Environments (ATEs) are deployed, which are specialized for and geared to fully automated high volume production test provided with powerful tools and universal Test Description Language (TDL) [6] for test development and debugging. Alternatively, for low volume DUT specific testing at low cost, the rack-and-stack (modular) ATE solutions are deployed while in case of a special approach the test development can be quite time consuming due to the lack of universal test development environment [7], [8]. Further, the build-in self-test is one other Design-for-Test

(DfT) approach, which provides the device with additional testability for verifying regarding to manufacturing defects. At this point, it should be noticed, that — as opposed to specification-oriented test — the "known" manufacturing defects are tested based on the underlying "failure model", e.g. the well known stuck-at failure and bridging fault, respectively [9]. Due to the ever increasing size and complexity of Very-Large-Scale-Integration (VLSI) designs, there is also an increasing demand for investigation of new approaches for the automatic test pattern generation (ATPG) for both test and diagnosis of faults [10].

Organization of the paper: In Section 2 a fail-safe combinational DUT structure is introduced and the corresponding data modeling is discussed. In Section 3 the challenge for localization of the so called dominated faults is discussed and the problem solution is presented. Further, the overall modeling of data, test and diagnose for single as well as multiple fault detection is claimed. Additionally, the implementation of the uATE is described. Finally the paper closes with a conclusion in Section 4.

2 Case Study: A Fail-Safe Structure

Let the DUT structure in **Fig.** 1 be given. VDD denotes the pin of the voltage power supply. A denotes the gate pin of the high-active transistor and the primary input pin of the DUT, respectively. R1, R2 and R3 denote the resistors with the resistance ratio

$$\frac{\mathrm{R1}}{\mathrm{R2}} = \frac{\mathrm{R1}}{\mathrm{R3}} = \frac{1}{10}\,.$$

2.1 Circuit Failure Modeling

In normal operation the serial jumpers J1 and J4 are plugged, termed as $\mathrm{J1} = 1$ and $\mathrm{J4} = 1$ or rather briefly J1 and J4 using the high-active notation. Accordingly, a modeled open circuit failure is done by unplugging the (normally plugged) respective jumper termed as $\mathrm{J1} = 0$ and $\mathrm{J4} = 0$ or rather briefly $\overline{\mathrm{J1}}$ and $\overline{\mathrm{J4}}$. And analogously, in normal operation the parallel jumpers $\overline{\mathrm{J2}}$ and $\overline{\mathrm{J3}}$ are unplugged, termed as $\overline{\mathrm{J2}} = 1$ and $\overline{\mathrm{J3}} = 1$ or rather briefly $\overline{\mathrm{J2}}$ and $\overline{\mathrm{J3}}$ using the low-active notation. Accordingly, a modeled short circuit failure is done by plugging the (normally unplugged) respective jumper termed as $\overline{\mathrm{J2}} = 0$ and $\overline{\mathrm{J3}} = 0$ or rather briefly $\overline{\overline{\mathrm{J2}}}$ and $\overline{\overline{\mathrm{J3}}}$. In addition, N denotes that the CMOS inverter exists and $\overline{\mathrm{N}}$ denotes that the CMOS inverter is missing.

2.2 Specification

The DUT is provided with two capture pins, AIN and AOUT. In case of $\mathrm{A} = 0$ the transistor is not conductive, thus AIN is assigned with digital 1 ($\mathrm{AIN} = 1$) and — after negation — AOUT is assigned with digital 0 ($\mathrm{AOUT} = 0$). And analogously, in case of $\mathrm{A} = 1$ the transistor is conductive, thus AIN is assigned with digital 0 ($\mathrm{AIN} = 0$) and — after negation — AOUT is assigned with digital 1 ($\mathrm{AOUT} = 1$). This is the very simple specification of the DUT, see **Table** 1.

Table 1: Simple specification of the DUT in Fig. 1

A	VDD	J1	$\overline{\mathrm{J2}}$	$\overline{\mathrm{J3}}$	J4	AIN	AOUT
0	1	1	1	1	1	1	0
1	1	1	1	1	1	0	1

2.3 Over-Current Protection

Obviously, in case of conductive input transistor ($\mathrm{A} = 1$) the resistor R1 limits the cross-current and protects against over-current, respectively. But it should be noticed, that in case of the short circuit defect $\overline{\overline{\mathrm{J3}}}$ and existing inverter N, if $\mathrm{AIN} = 0$ then the p-MOS transistor of the CMOS inverter conducts leading to the short circuit current. To prevent any damage, we deploy a current limited voltage power supply: On exceeding the specified current limit the voltage power supply switches to the over-current protection mode. In that case, the ATE connects VDD of the DUT to the ground so that VDD becomes defined 0V.

2.4 Defects

In case of the open circuit defect $\overline{\mathrm{J1}}$, the pull-down resistor R2 warrants that AIN is assigned with digital 0 ($\mathrm{AIN} = 0$) even in the case of $\mathrm{A} = 0$: this failure is termed as stuck-at 0 denoted as s@0. Similarly, in case of the short circuit defect $\overline{\overline{\mathrm{J2}}}$, AIN is connected to ground ($\mathrm{AIN} = 0$), which results in s@0 failure, too. Analogously, in case of the defects $\overline{\overline{\mathrm{J3}}}$, $\overline{\mathrm{J4}}$ and $\overline{\mathrm{N}}$, respectively, 0V is captured at AOUT ($\mathrm{AOUT} = 0$), which also results in s@0 failure.

It is remarkable, that in any modeled defect, the capture pins AIN and AOUT are designed to be assigned with a fail-safe signal level.

3 Enhanced Test Data Modeling

Section 2.4 makes clear that all of the defects result in s@0, so that they are not locatable separately. Hence, the question occurs, how to enhance the test accuracy. To surmount this challenge we deploy external current sources to provide additional stimuli at the given test points AIN and AOUT, see **Fig.** 2. $\overline{\mathrm{IS1}}$ and $\overline{\mathrm{IS2}}$ denote the first and the second current source, respective. Syntactically, $\overline{\mathrm{IS1}}$ and $\overline{\mathrm{IS2}}$ mean that both current sources are disabled, and $\overline{\overline{\mathrm{IS1}}}$ and $\overline{\overline{\mathrm{IS2}}}$ mean that both current sources are enabled.

3.1 Dominating vs. Dominated Faults

The use of external current sources leads to more varied test results, namely: In case of the single open circuit defect $\overline{\mathrm{J1}}$, the signal at AIN changes from 0 to 1 ($\mathrm{AIN} = 0 \rightarrow 1$) on enabling the first current source ($\overline{\mathrm{IS1}} = 1 \rightarrow 0$). Analogously, in case of the single open circuit defect $\overline{\mathrm{J4}}$, the signal at AOUT changes from 0 to 1 ($\mathrm{AOUT} = 0 \rightarrow 1$) on enabling the second current source ($\overline{\mathrm{IS2}} = 1 \rightarrow 0$).

Contrastingly, in case of the short circuit defect $\overline{\overline{\mathrm{J2}}}$, the signal at AIN still remains low on enabling the first current source. Analogously, in case of the short circuit defect $\overline{\overline{\mathrm{J3}}}$, the signal at AOUT still remains low on enabling the second current source.

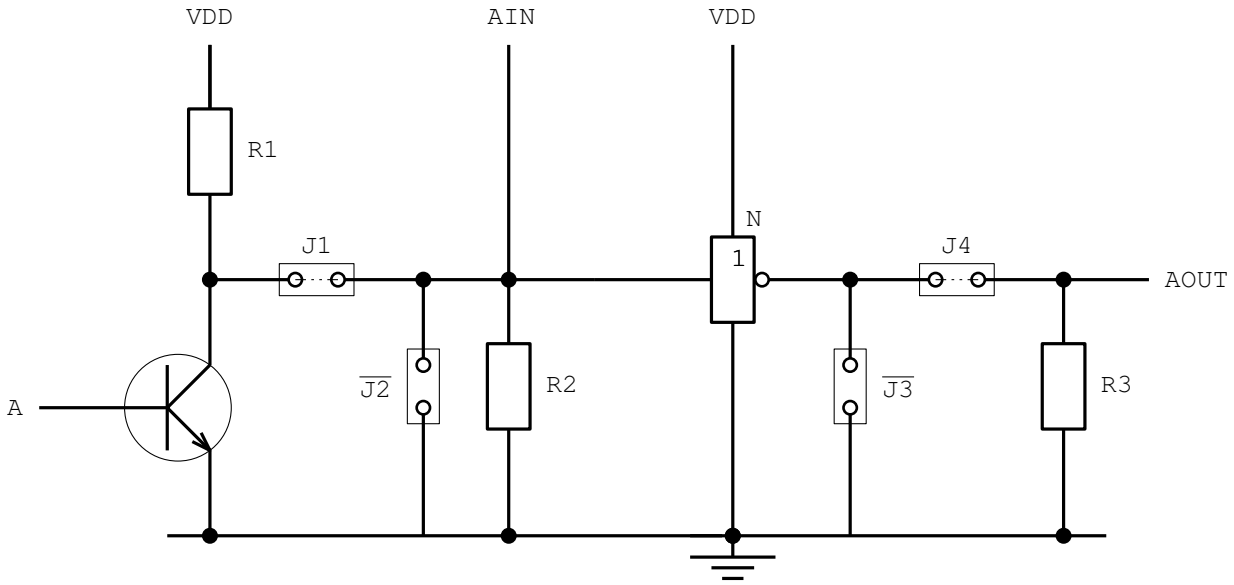


Fig. 1: Combinational fail-safe DUT structure

Obviously, one can notice that the short circuit defect dominates the open circuit defect. Thus, we are speaking of dominated faults $\overline{\texttt{J1}}$ and $\overline{\texttt{J4}}$ denoted as d@0; briefly, d@0 means "dominated by s@0".

3.2 Undefined Signal at AIN

The use of external current sources has its price also in data modeling: Let's say the over-current protection mode is activated (VDD $= 0$), the input pin A is assigned with 0 (A $= 0$) and the first current source is enabled ($\overline{\overline{\texttt{IS1}}}$). Then, due to the resistance ratio $\frac{\texttt{R1}}{\texttt{R2}} = \frac{1}{10}$, an analog voltage value is captured, which is neither a digital 1 nor a digital 0. In that case, AIN is modeled as undefined, symbolized with $*$: AIN $= *$.

3.3 Data Modeling

To create the overall data model, at first the encoding (header) is needed. It consists of the input vector x, the programing vector p and the output vector y. According to Fig. 2, the encoding of the part 1 is given as follows

- $x = (\texttt{A}, \overline{\texttt{IS1}}, \texttt{VDD})$
- $p = (\texttt{J1}, \overline{\texttt{J2}})$
- $y = (\texttt{AIN})$

and the encoding of the part 2 is given as follows

- $x = (\texttt{AIN}, \overline{\texttt{IS2}}, \texttt{VDD})$
- $p = (\overline{\texttt{J3}}, \texttt{J4}, \texttt{N})$
- $y = (\texttt{AOUT}, \texttt{VDD})$

Fig. 3 shows the corresponding block diagram, **Table** 2 shows the data model of part 1 and **Table** 3 shows the data model of part 2.

Each data model contains its overall modeling information about the test tree, the test flow and the diagnose flow for defect localization. For example, **Fig. 4 and 5** show the test tree of part 2 with VDD $= 1$ and VDD $= 0$, **Fig.** 6 shows the test flow of part 2 and **Fig. 7 and 8** shows the diagnose flow of part 2 with VDD $= 1$ and VDD $= 0$.

Table 2: Data model of part 1

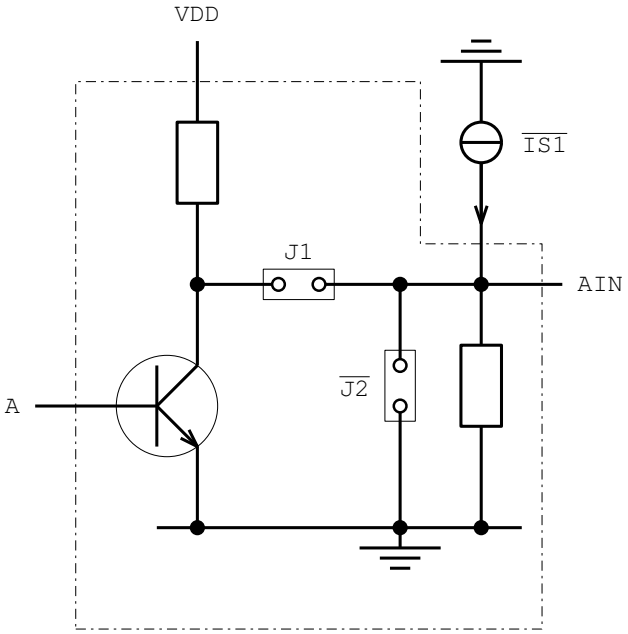
A	$\overline{\texttt{IS1}}$	VDD	J1	$\overline{\texttt{J2}}$	AIN	Comment
0	–	1	1	1	1	spec
1	–	1	1	1	0	
–	–	1	–	0	**0**	s@**0**
–	1	1	0	–	**0**	
–	0	1	0	1	**1**	d@**0**
–	1	0	1	1	0	spec
1	0	0	1	1	0	
0	0	0	1	1	$*$	undefined
–	–	0	–	0	**0**	s@**0**
–	1	0	0	–	**0**	
–	0	0	0	1	**1**	d@**0**

3.4 uATE in a Nutshell

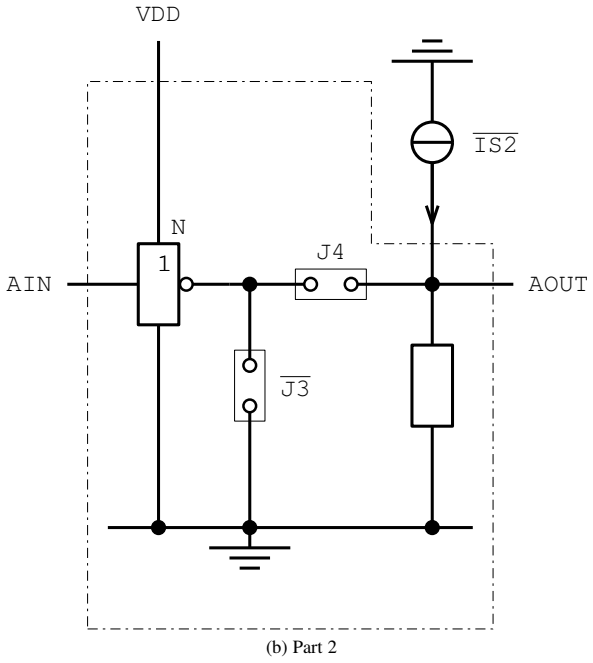
We deployed Arduino (Mega 2560) uC-Board to implement the uATE. Additionally, we used Raspberry Pi to implement the user interface for the test engineer as well as the client to program and control the uATE and for post processing, see **Fig.** 9.

We used the digital output port of the Arduino to source current to the respective data output pin of the DUT. To not overload the digital output port we equipped it with a diode and resistor to only source a limited current.

The test and diagnose flow was implemented by defining the initial test function and further defining the next test function depending on the branch code returned from the current test function. The program flow was required to maximize the test coverage on minimal use of external current sources (Resources) and minimal test time. The test automation was implemented by the firmware of the uC. The test program is developed in terms of a conventional ATE including the pin-mapping, the test function library and the test flow (schedule).



(a) Part 1



(b) Part 2

Fig. 2: External current sources to enhance the test accuracy

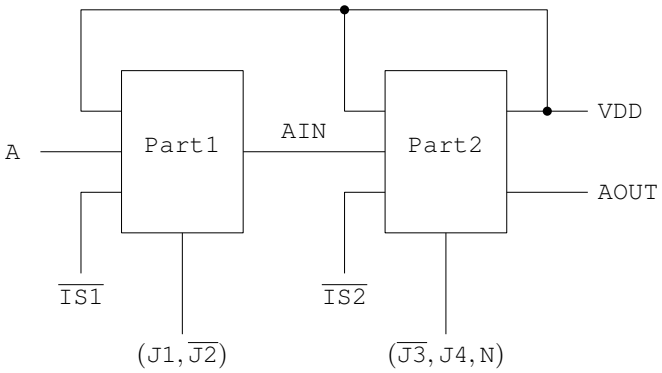


Fig. 3: Block diagram

Table 3: Data model of part 2

AIN	IS2	VDD	J3	J4	N	AOUT	VDD	Comment
0	1	1	1	1	1	1	1	spec
1	1	1	1	1	1	0	1	
–	1	1	–	–	0	**0**	1	s@**0**
–	1	1	1	0	–	**0**	1	
1	1	1	0	–	–	**0**	1	
0	1	1	0	–	1	**0**	**0**	
0	0	1	1	1	1	1	1	spec
1	0	1	1	1	1	0	1	
–	0	1	1	–	0	**1**	1	d@**0**
–	0	1	–	0	0	**1**	1	
1	0	1	–	0	–	**1**	1	
–	0	1	1	0	–	**1**	1	
0	0	1	0	0	1	**1**	**0**	d@**0**, s@**0**
0	0	1	0	1	1	**0**	**0**	
–	0	1	0	1	0	**0**	1	s@**0**
1	0	1	0	1	–	**0**	1	
–	1	0	1	1	1	0	0	spec
1	0	0	1	1	1	0	0	
0	0	0	1	1	1	1	0	
–	1	0	–	–	0	**0**	0	s@**0**
–	1	0	–	0	–	**0**	0	
–	–	0	0	1	–	**0**	0	
–	0	0	1	–	0	**1**	0	d@**0**
–	0	0	–	0	–	**1**	0	

4 Conclusion

In this work, the overall event-based data modeling for test and diagnose was presented. For this purpose, the DUT structure was decomposed in sub-structures. For each sub-structure the corresponding encoding was formulated. The structure was modeled as a block diagram and the data model was created.

Proceeding from the data model the corresponding test tree was derived. The test tree already provides a suitable representation of paths to deduce the test flow and the diagnose flow for defect localization. To enhance the test accuracy external current sources were deployed and the data modeling was upgraded. Accordingly, the enhanced test and diagnose flow were created. In doing so the minimization of test time and resources was pursued. Finally, in accordance with the data modeling, the test and diagnose flow were implemented as a firmware and a suitable uC-Board was implemented as a uATE. Thus, the feasibility was shown.

It is remarkable that the presented data modeling is not limited to single faults, but also takes multiple faults into consideration. Furthermore, it is remarkable that enhancing the test accuracy using current sources results in an additional DfT criterion and establishes the concept of dominated failure in contrast to the stuck-at failure. Working with our uATE can help to understand failure detection and fault localization in automotive safety critical circuits, and serves as a prototype for processor based self

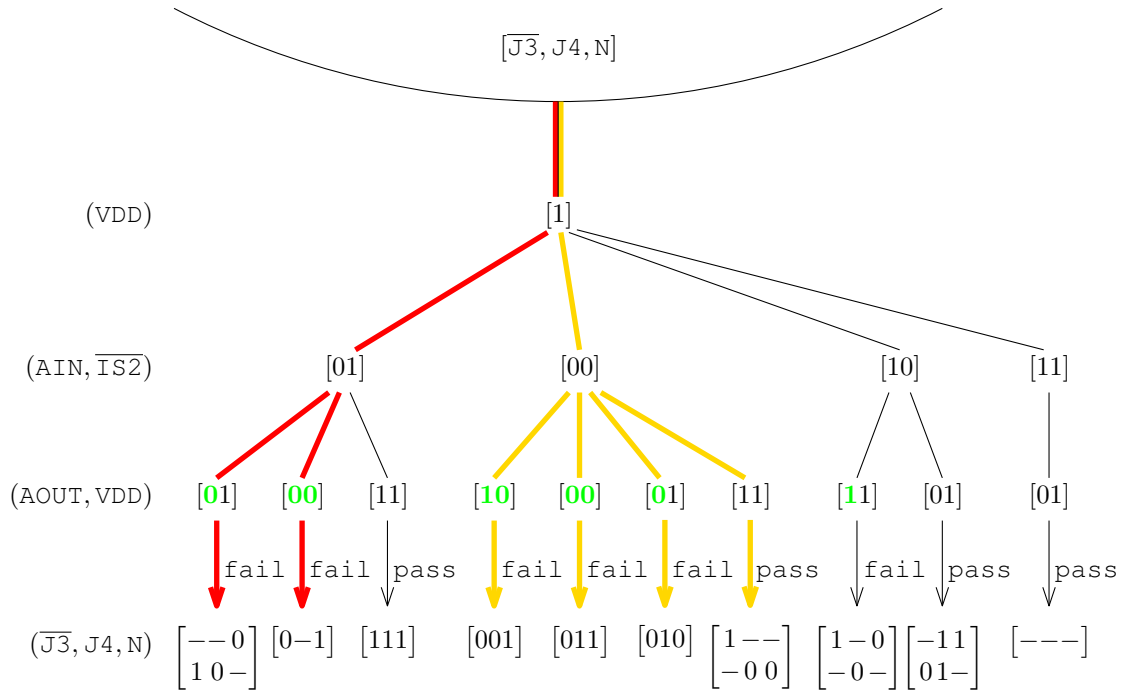


Fig. 4: Test tree of part 2 with VDD = 1

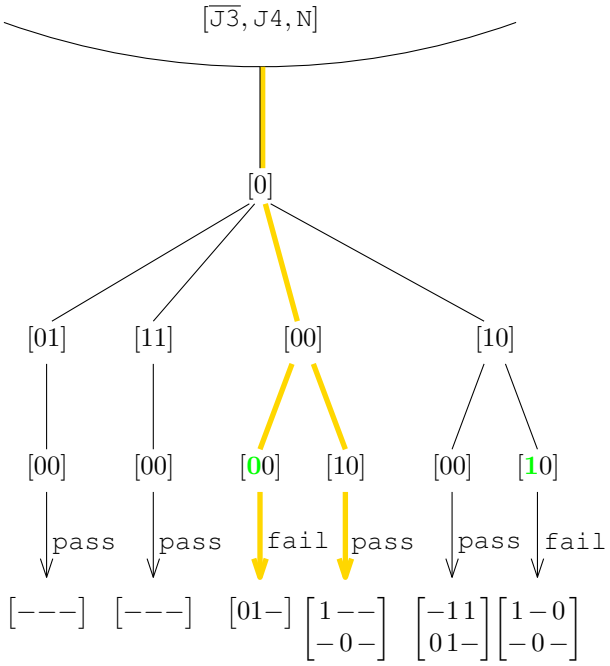


Fig. 5: Test tree of part 2 with VDD = 0

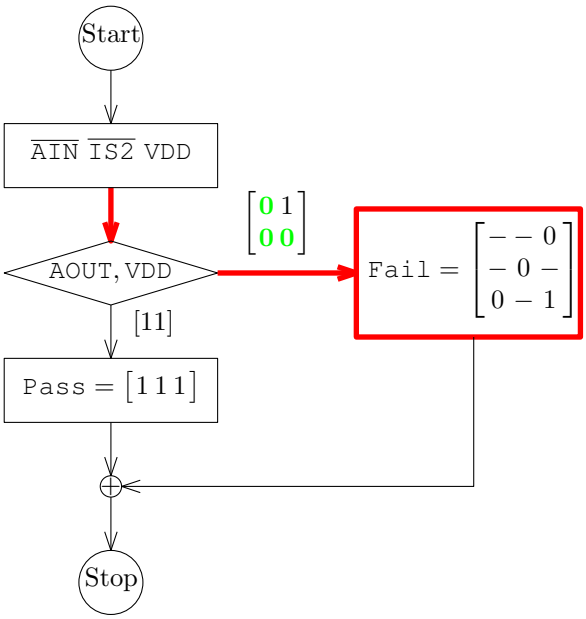


Fig. 6: Test flow of part 2

testing and diagnosis.

Outlook: The presented modeling is suitable for generating of algorithms for enhanced test and diagnosis (defect localization). Furthermore, the used data format TVL (Ternary Vector List [11], [12]) is suitable to handle big data on low-level and hardware implementation, respectively, providing maximal processing power and minimal memory requirements. Hence, it is obvious to automatically generate high performance algorithms for test and diagnosis based on the presented data modeling. At this point, the invertible decomposition of the given DUT structure using the automata based parallel composition [13] can additionally provide "divide and conquer" and hence this can result in further reduction of complexity.

Acknowledgement: We express our thanks to Dr. Benjamin Cella, Dr. Michael Schmidt and Dr. Alfred Engler from Liebherr-Elektronik GmbH for inspiring and fruitful discussions and the provision of the PCB.

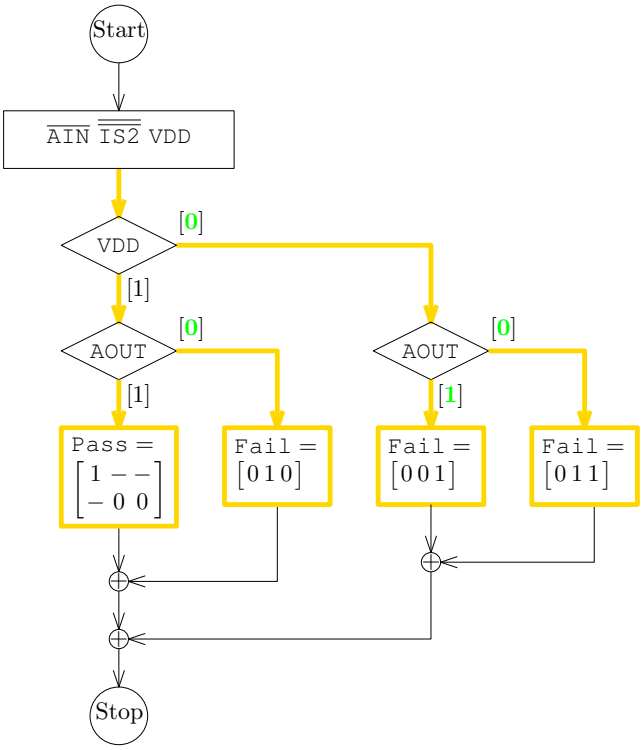


Fig. 7: Diagnose flow of part 2 with VDD = 1

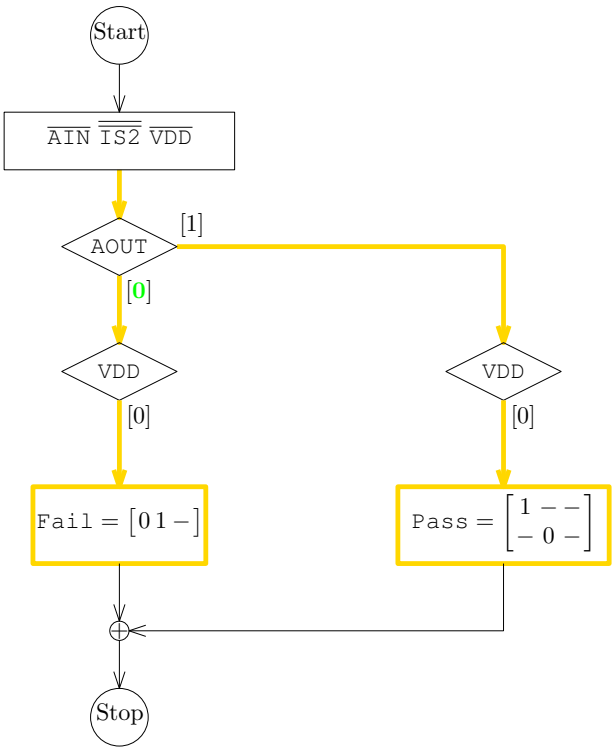


Fig. 8: Diagnose flow of part 2 with VDD = 0

References

[1] *Automotive IC Market to Display Strongest Growth Through 2018, IC INSIGHTS (November 18, 2014).*

[2] D. Foty, "The future of "Moore's Law" - Does it have one?" in *Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2015 International Conference on*, Sept 2015.

[3] Y. Xu, "Algorithms for automatic generation of relative timing constraints," Ph.D. dissertation, Salt Lake City, UT, USA, 2011.

[4] R. P. Kurshan and K. L. McMillan, "Analysis of digital circuits through symbolic reduction," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 10, no. 11, pp. 1356–1371, 1991.

[5] T. Yoneda, T. Kitai, and C. J. Myers, "Automatic derivation of timing constraints by failure analysis," in *CAV*, ser. Lecture Notes in Computer Science, E. Brinksma and K. G. Larsen, Eds., vol. 2404. Springer, 2002, pp. 195–208.

[6] *Advantest Corporation, "Viewpoint TDL Programming Manual", Manual No. 8262578-19 , Vol 1., November 2001.*

[7] A. Kafton, "Advanced Technology Speeds RF-Integrated-Circuit Testing," *ARFTG Conference Digest-Fall, 46th*, vol. 28, pp. 104–113, Nov. 1995.

[8] R. Smith, D. Rosenthal, and S. Stevens, "Hybrid Modular Test System Architectures," *AUTOTESTCON, 2006 IEEE*, pp. 658–658, Sept. 2006.

[9] Y.-R. Shieh and C.-W. Wu, "Design of cmos pscd circuits and checkers for stuck-at and stuck-on faults," *VLSI Design*, vol. 5, no. 4, pp. 357–372, 1998.

[10] P. Raiola, J. Burchard, F. Neubauer, D. Erb, and B. Becker, "Evaluating the effectiveness of d-chains in sat-based atpg and diagnostic tpg," *Journal of Electronic Testing*, vol. 33, no. 6, pp. 751–767, Dec 2017.

[11] Dieter Bochmann and Bernd Steinbach, *Logikentwurf mit XBOOLE.* Verlag Technik Berlin, 1991.

[12] C. Posthoff and B. Steinbach, *Logic Functions and Equations: Binary Models for Computer Science.* Boston, MA: Springer US, 2004, ch. Logic Functions and Equations, pp. 37–89.

[13] Gürkan Uygur and Sebastian Sattler, "A New Approach for Modeling Inconsistencies in Digital-Assisted Analog Design," *Journal of Electronic Testing*, vol. 32, no. 4, pp. 491–503, 2016.

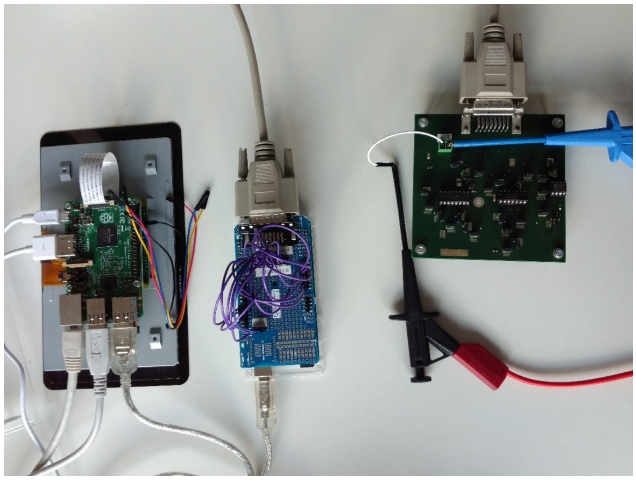


Fig. 9: Components of the uATE: Raspberry Pi, Arduino, DUT